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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/639,915	08/16/2000	Wilson P. Snyder II	9215/021	4050

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EXAMINER	
SCHEIBEL, ROBERT C	

ART UNIT	PAPER NUMBER
2666	10

DATE MAILED: 06/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/639,915	SNYDER ET AL.	
	Examiner	Art Unit	
	Robert C. Scheibel	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 3/17/04

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-15 and 17-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-15 and 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see lines 4-8 of page 7, filed March 19, 2004, with respect to the rejection of claims 5, 15, 7-9, and 17-19 have been fully considered but they are not persuasive. Regarding claims 5, 8-9, 15, and 19, the previous rejection under 35 U.S.C 112 has been overcome and the rejection of these claims has been withdrawn. However, claims 7 and 17-18 are still rejected under 35 U.S.C. 112 for reasons similar to the original rejection. Suggestions for overcoming these rejections are included in the detailed rejection below.

2. Applicant's arguments, see lines 9-21 of page 7, filed March 19, 2004, with respect to the rejection of claims 1 and 11 under 35 U.S.C. 102(e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new grounds of rejection is made in view of the fact that the amended claims 1 and 11 are obvious in view of the prior art as described in the rejection under 35 U.S.C. 103(a) below. Further, the amended claims are now subject to an obviousness double-patenting rejection over application 09/640,231 as described in detail below.

Applicant asserts that U.S. Patent U.S. 6,373,846 to Daniel, et al fails to disclose the limitation of a co-processor that contains context buffers. However, Daniel does disclose a co-processor comprising a plurality of context buffers in the combination of the EDMA and APU memory. Daniel fails to disclose the limitation of the context buffers

having an in-use counter. However, as explained below, this limitation is obvious in view of EP 0 710 046 to Byrn, et al. Applicant further remarks that U.S. Patent 6,311,212 to Chong et al stores context information for only some of the packets, specifically, the most recently used VCs. Applicant states that this is different than the present invention, as the core processor may have to wait in some instances to fetch the VC descriptor from off-chip memory. Examiner agrees with this characterization of Chong; however, the claim language is broad, only requiring that the co-processor automatically store the scheduling parameters. This broad language is disclosed in Chong as described below. However, the claim can be amended to overcome this rejection by distinguishing (in the claim language) the present invention from Chong's method of caching context information.

3. Additionally, applicant was silent with regard to the presumption of common ownership of each of the claims (see page 9 of the original office action (paper number 8). Applicant is reminded of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made. The examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims **1-4, 10-14, and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,373,846 to Daniel et al in view of U.S. Patent 6,311,212 to Chong and in further view of EP 0 710 046 to Byrn et al.

Regarding claims **1 and 11**, Daniel discloses an integrated circuit ***(element 32 in figure 2, column 11, lines 18-19 "single-chip integrated circuit device 32")*** that processes a communication packet ***(column 11, lines 31-34)***, the integrated circuit comprising:

a core processor ***(APU 36)*** configured to execute a software application that directs the core processor to process the communication packet ***(column 11, lines 53-61 "The power of the ATMCSI/TU 32 comes from the inclusion within the chip of a user-programmable RISC central processing unit (referred to herein as a APU, or ATM processing unit). For this APU, user-selected firmware may be downloaded to the on-chip APU during a system reset, and controls most of the operational***

aspects of the ATMCSI/TU 32. That is, the APU 36 exercises executive control over the operations of most of the other elements in the ATMCSI/TU 32."); and

scheduling circuitry ***(Timer Unit 44 together with Scheduler Unit 46 in figure 2; this combination is referred to a the "time management team" (see column 34, lines 45-46))*** configured to retrieve first scheduling parameters cached in a context buffer for the packet ***(column 22, lines 13-16 "the scheduler 46 makes a request over a bus ... to obtain the first word of the given VCD"; the VCD is the context buffer which contains scheduling parameters such as the class field (see figure 7))*** and execute a first algorithm based on the first scheduling parameters to schedule subsequent transmission of the communication packet ***(column 35, lines 21-24 "the ATMCSI/TU 32, via the scheduler 46, implements a modified algorithm which computes a variable time interval in the future at which a cell transmission should next be scheduled")***.

Daniel further discloses a co-processor **(the combination of EDMA 40 and APU memory 38 of Figure 2 and described as such in lines 20-21 of column 13 "The EDMA unit 40 is effectively a coprocessor under control of the APU 16")**, comprising a plurality of context buffers **(VCDs and BFDs described in lines 33-39 of column 14)** for storing context associated with events **(receiving the CS-PDUs)**.

Daniel does not disclose expressly the limitation of the context buffers having an in-use counter, or the limitation of the co-processor automatically storing the scheduling parameters in the context buffer.

Chong discloses the limitation of the co-processor automatically storing the scheduling parameters in the context buffer ***(see the abstract which teaches caching of VCDs which contain scheduling parameters "the single-chip network processor includes an on-chip cache memory that stores VC descriptors for fast retrieval")***.

Daniel and Chong are analogous art because they are from the same field of endeavor of integrated circuits used in ATM switching.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Daniel by caching the VCDs. The motivation for doing so would have been to "enhance system performance" because "VCs are stored to the cache and retrieved much quicker from the cache than from the off-chip memory" as suggested in the abstract of Chong.

Daniel, as modified by Chong above, does not disclose expressly the limitation of the context buffers having an in-use counter.

Byrn discloses the limitation of the context buffers having an in-use counter in the queue length QL 33 of figure 3. The queue length tracks the number of cells associated with the given VC.

Daniel, Chong, and Byrn are analogous art because they are from the same field of endeavor of data communications systems. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Chong (as modified above) to track the usage of the context buffers to indicate when they can be moved back to external memory. The motivation for so doing is to improve performance by not

processing inactive context buffers as suggested in lines 14-17 of column 3. Therefore it would have been obvious to combine Daniel and Chong with Byrn to obtain the invention as specified in claims 1 and 11.

Regarding claims **2 and 12**, in column 7, lines 9-11, Daniel discloses "multiple simultaneous algorithms may be run so that flow control may be determined by a selected or most advantageous method". This anticipates simultaneously running a second algorithm. Since Daniel teaches reading scheduling information as taught in the rejection above, it follows that the second algorithm would be implemented similarly by read scheduling information. Further, column 29, lines 35-40 indicate that the flow control algorithms discussed in Daniel are determining which VC to service next and are thus scheduling algorithms.

Regarding claims **3 and 13**, Daniel discloses integrated circuit of claim 2 wherein the first algorithm and the second algorithm comprise guaranteed cell rate algorithms ***(see column 34, lines 56-58 "the class of service known as variable-bit-rate service is usually used to transmit compressed video images without delay"; the modified GCRA algorithm described in column 35, lines 21-36 handles this type of traffic – since this algorithm is transmitting video, it is certainly referring to real-time VBR traffic and as such it guarantees a cell rate).***

Regarding claims **4 and 14**, Daniel discloses the integrated circuit of claim 1 wherein scheduling circuitry is configured to update the first scheduling parameters and write the updated scheduling parameters to the context buffer ***(see column 35, line***

36 through column 36, line 2; the parameters described here are used in scheduling and are updated as described (for example, the LCT time)).

Regarding claims **10 and 20**, Daniel discloses the integrated circuit of claim 1 wherein the scheduling circuitry is configured to operate in parallel with the core processor ***(see figure 2 indicates "the time management team" (timer unit 44 and scheduler unit 46) operating in parallel with the core processor (APU 36))***.

7. Claims **5 and 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,373,846 to Daniel et al in view of U.S. Patent 6,311,212 to Chong and in further view of EP 0 710 046 to Byrn et al as applied to claims 1 and 11 above, and in further view of U.S. Patent 6,205,150 to Ruszczyk.

Daniel, as modified above, discloses the limitations of the parent claims 1 and 11 as discussed above.

Daniel, as modified, does not disclose expressly the limitations found in claims 5 and 15 of attempting to schedule with a second (lower) priority and then attempting with a first (higher) priority if unsuccessful.

Ruszczyk discloses integrated circuit of claim 1 wherein the first scheduling parameters indicate a first one of the priority levels ***(the priority of the high priority queue 62)*** and a second one of the priority levels ***(the priority of the low priority queue 66)***, wherein the first priority level has a higher priority than the second priority level, and wherein the scheduling circuitry is configured to first attempt to schedule the transmission of the communication packet with the second priority level ***(column 6,***

lines 13-16 "Router 20 then schedules the lower priority data packet in low priority queue 66 using a weighted round robin scheduling method scheduler 68"), and if unsuccessful, then to attempt to schedule the transmission of the communication packet with the first priority level ***(column 6, lines16-20 "Once a transmission deadline of a lower priority data packet in low priority queue 66 has expired, a promoter 70 promotes the lower priority data packet to high priority queue 62 whereby the promoted data packet is scheduled by guaranteed scheduling method 64"; the expiration of the transmission deadline is the determination that the attempt at the second priority level is unsuccessful)***.

Daniel, as modified, and Ruszczyk are analogous art because they are from same field of endeavor of packet scheduling.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Daniel, as modified above, to use a transmission deadline and to promote the priority of a packet from a lower to a higher priority when the transmission deadline expired at the lower priority.

The motivation for doing so is suggested in the abstract of Ruszczyk "This method ensures that lower priority data packets are not starved out of delayed in execution by higher priority data packets".

Therefore, it would have been obvious to combine Ruszczyk with Daniel, as modified, for the benefit of preventing the starvation of lower priority packets to obtain the invention as specified in claims 5 and 15.

8. Claims **7-9 and 17-19** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,373,846 to Daniel et al in view of U.S. Patent 6,311,212 to Chong and in further view of EP 0 710 046 to Byrn et al as applied to claims 1 and 11 above, and further in view of U.S. Patent 6,327,246 to Jones.

Daniel, as modified, discloses the limitations of the parent claims 1 and 11 as described above.

Daniel, as modified, does not disclose expressly the limitation of a highest priority level being for CBR traffic (claims 7 and 17), a lowest priority level being for ABR traffic (claims 8 and 18), or a first priority being for real-time traffic and a second priority being for non-real-time traffic (claims 9 and 19).

Regarding claims 7 and 17, Jones discloses a highest one of the priority levels is for scheduling constant bit rate traffic ***(column 1, line 67 through column 2 line 3 "These include "constant bit rate" (CBR) service, which is the highest priority level...")***.

Regarding claims 8 and 18, Jones discloses a highest one of the priority levels is for scheduling constant bit rate traffic ***(column 1, line 67 through column 2 line 3 "...and available bit rate (ABR) service, which is the lowest priority level")***.

Regarding claims 9 and 19, Jones discloses a first one of the priority levels is for scheduling real-time traffic, a second one of the priority levels is for scheduling non-real-time traffic, and wherein the first priority level has a higher priority than the second priority level ***(column 1, line 67 through column 2 line 3 "These include "constant bit rate" (CBR) service, which is the highest priority level, two "variable bit rate"***

(VBR) services, and available bit rate (ABR) service, which is the lowest priority level"; it is well known that the CBR service is used for real-time traffic and the ABR service is used for non-real-time traffic).

Daniel, as modified, and Jones are analogous art because they are from the same field of endeavor of ATM switching.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Daniel, as modified above, to explicitly handle the 4 services (CBR, 2 VBRs, and ABR) according to the priority hierarchy indicated in Jones.

The motivation for doing so would have been to properly "handle the cells according to their priority levels" as provided for in the ATM standard as suggested in Jones from column 1, line 65 through column 2, line 5.

Therefore, it would have been obvious to combine Jones with Daniel, as modified, for the benefit of handling cells according to their priority to obtain the invention as specified in claims 7-9 and 17-19.

Double Patenting

9. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

10. Claims **1-4, 10-14, and 20** are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 11 of copending Application No. 09/640,231 in view of U.S. Patent 6,373,846 to Daniel et al and in further view of U.S. Patent 6,311,212 to Chong.

Regarding claims 1 and 11 of the instant application claims 1 and 11 of copending application 09/640,231 disclose the limitations of a core processor in the similarly worded limitation. The various co-processor limitations of claims 1 and 11 of copending application 09/640,231 further disclose the limitations a co-processor.

Claims 1 and 11 of copending application 09/640,231 fail to disclose the limitation of scheduling circuitry.

Daniel discloses scheduling circuitry ***(Timer Unit 44 together with Scheduler Unit 46 in figure 2; this combination is referred to a the "time management team" (see column 34, lines 45-46))*** configured to retrieve first scheduling parameters cached in a context buffer for the packet ***(column 22, lines 13-16 "the scheduler 46 makes a request over a bus ... to obtain the first word of the given VCD"; the VCD is the context buffer which contains scheduling parameters such as the class field (see figure 7))*** and execute a first algorithm based on the first scheduling parameters to schedule subsequent transmission of the communication packet ***(column 35, lines 21-24 "the ATMCSI/TU 32, via the scheduler 46, implements a modified***

algorithm which computes a variable time interval in the future at which a cell transmission should next be scheduled").

Copending application 09/640,231 and Daniel are analogous art because they are from the same field of endeavor of integrated circuits used in ATM switching.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify copending application 09/640,231 to add scheduling circuitry. The motivation for doing so would have been to free the core processor (APU) from doing some repetitive tasks, thus allowing the core processor (APU) to perform supervisory tasks and the actual communication of digital data packets as specified in the abstract of Daniel.

However, copending application 09/640,231 and Daniel do not disclose expressly the limitation of the co-processor automatically storing the scheduling parameters in the context buffer.

Chong discloses the limitation of the co-processor automatically storing the scheduling parameters in the context buffer ***(see the abstract which teaches caching of VCDs which contain scheduling parameters "the single-chip network processor includes an on-chip cache memory that stores VC descriptors for fast retrieval")***.

Copending application 09/640,231, Daniel and Chong are analogous art because they are from the same field of endeavor of integrated circuits used in ATM switching.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Daniel by caching the VCDs. The motivation for doing so would

have been to "enhance system performance" because "VCs are stored to the cache and retrieved much quicker from the cache than from the off-chip memory" as suggested in the abstract of Chong.

Therefore, it would have been obvious to combine Chong with copending application 09/640,231, as modified by Daniel, for the benefit of enhancing system performance to obtain the invention as specified in claims 1 and 11.

Regarding claims **2 and 12**, in column 7, lines 9-11, Daniel discloses "multiple simultaneous algorithms may be run so that flow control may be determined by a selected or most advantageous method". This anticipates simultaneously running a second algorithm. Since Daniel teaches reading scheduling information as taught in the rejection above, it follows that the second algorithm would be implemented similarly by read scheduling information. Further, column 29, lines 35-40 indicate that the flow control algorithms discussed in Daniel are determining which VC to service next and are thus scheduling algorithms.

Regarding claims **3 and 13**, Daniel discloses integrated circuit of claim 2 wherein the first algorithm and the second algorithm comprise guaranteed cell rate algorithms ***(see column 34, lines 56-58 "the class of service known as variable-bit-rate service is usually used to transmit compressed video images without delay"; the modified GCRA algorithm described in column 35, lines 21-36 handles this type of traffic – since this algorithm is transmitting video, it is certainly referring to real-time VBR traffic and as such it guarantees a cell rate).***

Regarding claims **4 and 14**, Daniel discloses the integrated circuit of claim 1 wherein scheduling circuitry is configured to update the first scheduling parameters and write the updated scheduling parameters to the context buffer ***(see column 35, line 36 through column 36, line 2; the parameters described here are used in scheduling and are updated as described (for example, the LCT time))***.

Regarding claims **10 and 20**, Daniel discloses the integrated circuit of claim 1 wherein the scheduling circuitry is configured to operate in parallel with the core processor ***(see figure 2 indicates "the time management team" (timer unit 44 and scheduler unit 46) operating in parallel with the core processor (APU 36))***.

It would have been obvious to one of ordinary skill in the art to modify copending application 09/640,231, as modified above, to include the limitations of claims 2-4, and 10 as taught by Daniel. The motivation for doing so would have been as above, to free the core processor (APU) from doing some repetitive tasks, thus allowing the core processor (APU) to perform supervisory tasks and the actual communication of digital data packets as specified in the abstract of Daniel. Therefore, it would have been obvious to combine Daniel with copending application 09/640,231, as modified, for the benefit of offloading some of the processing from the core processor to obtain the invention as specified in claims 2-4, 10-14, and 20.

This is a provisional obviousness-type double patenting rejection.

11. Claims **5 and 15** are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 11 of

copending Application No. 09/640,231 in view of U.S. Patent 6,373,846 to Daniel et al and in further view of U.S. Patent 6,311,212 to Chong and in further view of U.S. Patent 6,205,150 to Ruszczyk.

Copending application 09/640,231, as modified above, discloses the limitations of the parent claims 1 and 11 as discussed above.

Copending application 09/640,231, as modified, does not disclose expressly the limitations found in claims 5 and 15 of attempting to schedule with a second (lower) priority and then attempting with a first (higher) priority if unsuccessful.

Ruszczyk discloses integrated circuit of claim 1 wherein the first scheduling parameters indicate a first one of the priority levels ***(the priority of the high priority queue 62)*** and a second one of the priority levels ***(the priority of the low priority queue 66)***, wherein the first priority level has a higher priority than the second priority level, and wherein the scheduling circuitry is configured to first attempt to schedule the transmission of the communication packet with the second priority level ***(column 6, lines 13-16 "Router 20 then schedules the lower priority data packet in low priority queue 66 using a weighted round robin scheduling method scheduler 68")***, and if unsuccessful, then to attempt to schedule the transmission of the communication packet with the first priority level ***(column 6, lines16-20 "Once a transmission deadline of a lower priority data packet in low priority queue 66 has expired, a promoter 70 promotes the lower priority data packet to high priority queue 62 whereby the promoted data packet is scheduled by guaranteed***

scheduling method 64"; the expiration of the transmission deadline is the determination that the attempt at the second priority level is unsuccessful).

Copending application 09/640,231, as modified, and Ruszczyk are analogous art because they are from same field of endeavor of packet scheduling.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Copending application 09/640,231, as modified above, to use a transmission deadline and to promote the priority of a packet from a lower to a higher priority when the transmission deadline expired at the lower priority.

The motivation for doing so is suggested in the abstract of Ruszczyk "This method ensures that lower priority data packets are not starved out of delayed in execution by higher priority data packets".

Therefore, it would have been obvious to combine Ruszczyk with Copending application 09/640,231, as modified, for the benefit of preventing the starvation of lower priority packets to obtain the invention as specified in claims 5 and 15.

This is a provisional obviousness-type double patenting rejection.

12. Claims **7-9 and 17-19** are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 11 of copending Application No. 09/640,231 in view of U.S. Patent 6,373,846 to Daniel et al and in further view of U.S. Patent 6,311,212 to Chong and further in view of U.S. Patent 6,327,246 to Jones.

Copending Application No. 09/640,231, as modified, discloses the limitations of the parent claims 1 and 11 as described above.

Copending Application No. 09/640,231, as modified, does not disclose expressly the limitation of a highest priority level being for CBR traffic (claims 7 and 17), a lowest priority level being for ABR traffic (claims 8 and 18), or a first priority being for real-time traffic and a second priority being for non-real-time traffic (claims 9 and 19).

Regarding claims 7 and 17, Jones discloses a highest one of the priority levels is for scheduling constant bit rate traffic ***(column 1, line 67 through column 2 line 3 "These include "constant bit rate" (CBR) service, which is the highest priority level...")***.

Regarding claims 8 and 18, Jones discloses a highest one of the priority levels is for scheduling constant bit rate traffic ***(column 1, line 67 through column 2 line 3 "...and available bit rate (ABR) service, which is the lowest priority level")***.

Regarding claims 9 and 19, Jones discloses a first one of the priority levels is for scheduling real-time traffic, a second one of the priority levels is for scheduling non-real-time traffic, and wherein the first priority level has a higher priority than the second priority level ***(column 1, line 67 through column 2 line 3 "These include "constant bit rate" (CBR) service, which is the highest priority level, two "variable bit rate" (VBR) services, and available bit rate (ABR) service, which is the lowest priority level"; it is well known that the CBR service is used for real-time traffic and the ABR service is used for non-real-time traffic)***.

Copending Application No. 09/640,231, as modified, and Jones are analogous art because they are from the same field of endeavor of ATM switching.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Copending Application No. 09/640,231, as modified above, to explicitly handle the 4 services (CBR, 2 VBRs, and ABR) according to the priority hierarchy indicated in Jones.

The motivation for doing so would have been to properly "handle the cells according to their priority levels" as provided for in the ATM standard as suggested in Jones from column 1, line 65 through column 2, line 5.

Therefore, it would have been obvious to combine Jones with Copending Application No. 09/640,231, as modified, for the benefit of handling cells according to their priority to obtain the invention as specified in claims 7-9 and 17-19.

This is a provisional obviousness-type double patenting rejection.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert C. Scheibel whose telephone number is 703-305-9062. The examiner can normally be reached on 6:30-3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema S. Rao can be reached on 703-308-5463. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RCS 5-24-04

Robert C. Scheibel
Examiner
Art Unit 2666

Seema S. Rao

SEEMA S. RAO 5/25/04
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